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06EC4

Fourth Semester B.E. Degree Examination, June/July 08
Fundamentals of VHDL

Time: 3 hrs. Max. Marks:10(

Note : ***Answer any FIVE full questions choosing at least TWO from each Part.***

Part – A

1 a. Explain how data types are classified in HDL. Mention the advantages of VHDL data types over verilog. **(06 Marks)**

b. Write behavioral description of the circuit of Fig.1(b) using VHDL. **(06 Marks)**

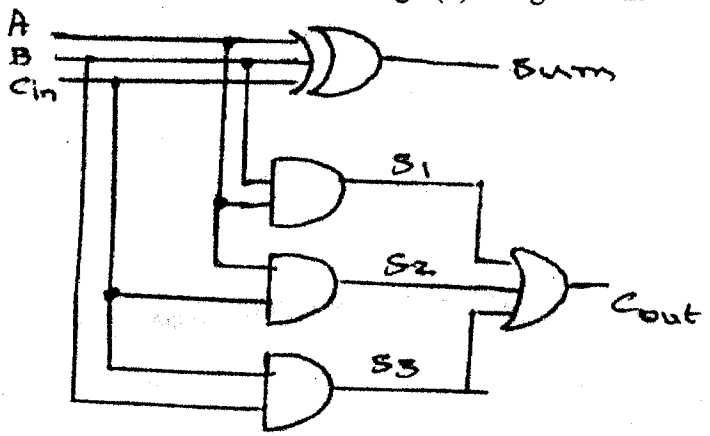


Fig.1(b)

c. For the inverter circuit of Fig.1(c) write switch level description in verilog. Explain the advantage of this type description over the other type. **(08 Marks)**

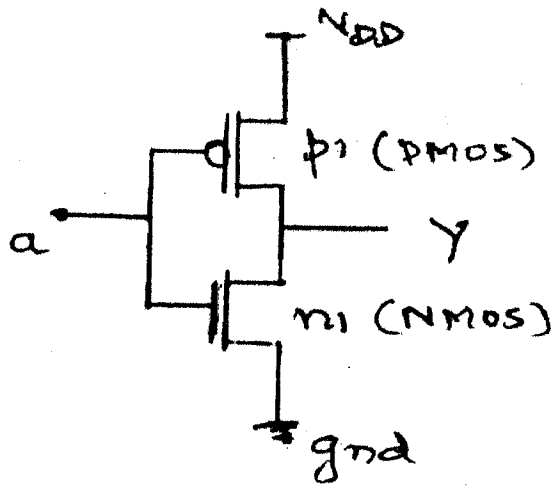
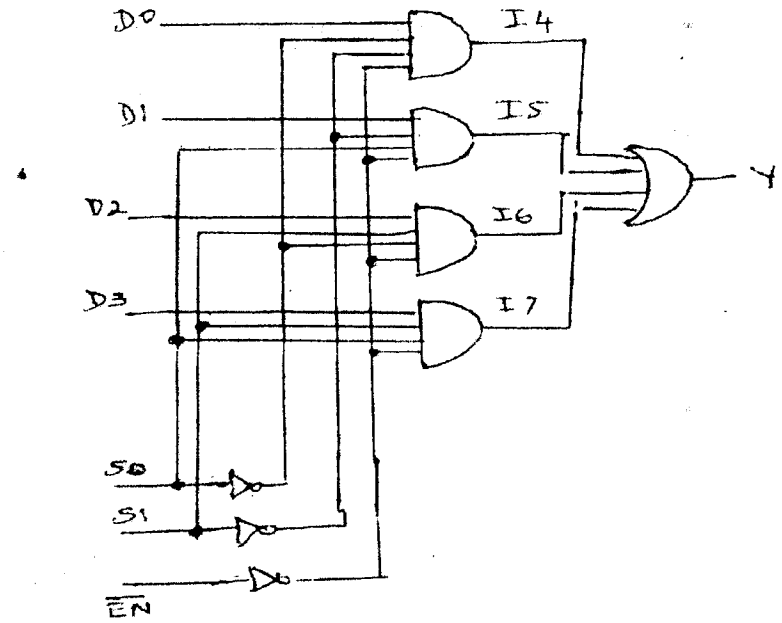


Fig.1(c)

2 a. With illustrations briefly discuss
   i) Signal declaration and assignment statements
   ii) Concurrent signal assignment statements and
   iii) Constant declaration and assignment statements. **(09 Marks)**

b. For the multiplexer circuit of Fig.2(b), write signal declaration and assignment statements in VHDL. Assume 10 nsec as propagation delay. Write your comments wherever it is applicable. (06 Marks)



4 × 1 multiplexer

Fig.2(b)

c. Explain how an object that has a width of more than 1 bit is declared in HDL using vector data types. Give examples. (05 Marks)

3 a. Write behavioral description of half adder in VHDL and verilog with propagation delay of 5 nsec. Discuss the important features of their description in VHDL and verilog. (08 Marks)

b. Explain the structure of various loop statements in HDL with examples. (12 Marks)

4 a. What is binding? Discuss binding between
   i) Entity and architecture
   ii) Entity and components and
   iii) Binding between library and module in VHDL with examples. (09 Marks)

b. Write complete VHDL description for full adder using two half adders. Explain how binding is incorporated with half adder. (11 Marks)

Part – B

5 a. Explain the following syntax with examples :
   i) Procedure ii) Task and iii) Function (08 Marks)

b. Write VHDL description of an N bit ripple carry adder using procedure. (12 Marks)

6 a. Describe all file processing procedures in VHDL with examples. (08 Marks)

b. Why mixed type description is needed? Explain (04 Marks)

c. Write a VHDL code for finding largest element of an array. (08 Marks)

7 a. How to invoke a verilog module from VHDL module? Write a mixed language description of an 'OR' gate where VHDL code invokes the verilog module 'OR3' (3 input OR gate). (10 Marks)

b. Write a mixed language description of a 4 bit adder with zero flag. (10 Marks)

8 a. What are the limitations of mixed language description? (05 Marks)

b. Discuss some of the important facts related to synthesis. (07 Marks)

c. Discuss synthesis information from entity with examples. (08 Marks)

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06EC45

Fourth Semester B.E. Degree Examination, June-July 2009
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions selecting at least TWO from each part.*

PART – A

1 a. Write the result of all shift and rotate operations in VHDL after applying them to a 7 bit vector A = 1001010. **(06 Marks)**

b. Explain composite and Access data types with an example for each. **(08 Marks)**

c. Mention different styles (types) of descriptions. Explain mixed type and mixed language descriptions. **(06 Marks)**

2 a. How do you assign delay to a signal assignment statement? Explain with an example in VHDL and verilog. **(04 Marks)**

b. What is a vector? Give an example for VHDL and verilog vector data types. **(04 Marks)**

c. With the help of a truth table and K-maps write Boolean expression for a 2-bit magnitude comparator. Write VHDL / verilog code **(12 Marks)**

3 a. Write VHDL code for a D-latch using variable assignment and signal assignment statements. With simulation waveforms clearly distinguish between the 2 statements. **(10 Marks)**

b. Explain verilog Repeat and Forever statements with an example. **(04 Marks)**

c. Write verilog code for a 4-bit counter with synchronous hold. **(06 Marks)**

4 a. What is binding? Discuss binding between two modules in verilog. **(06 Marks)**

b. Write VHDL behavioral description of a tristate buffer. Use this as a component for structural description of a 2 to 4 decoder with tristate output. **(10 Marks)**

c. Explain the use of Generic (in VHDL) and parameter (in verilog) with an example. **(04 Marks)**

PART – B

5 a. Write verilog code to convert a signed binary to Integer using task. **(08 Marks)**

b. Write VHDL / verilog function to find greater of 2 signed numbers. **(04 Marks)**

c. Table Q.5(c) below shows a file containing real numbers. Write a VHDL code for reading the file, multiply the first number by 2, second by 5, third by 3 and fourth by 4. The products to be stored in real variables z, z1, z2 and z3 respectively. **(08 Marks)**

-13.4 -5.564 0.23
-55.32

Table Q.5(c) File file _ real . txt

6 a. Write a note on packages in VHDL. **(05 Marks)**

b. Write VHDL code for addition of two 5 x 5 matrices using a package. **(07 Marks)**

c. Write the block diagram and function table of a SRAM. Using these, write a verilog description for 16 x 8 SRAM. **(08 Marks)**

7 a. How to invoke a verilog module from a VHDL module? Explain with an example of a mixed language description for a full adder using 2 half adders. **(10 Marks)**

b. Write a mixed language description of a 9-bit adder consisting of three 3-bit carry-look ahead adders to show how a verilog module invokes VHDL entity. **(10 Marks)**

8 a. Explain extraction of synthesis information from Entity. **(04 Marks)**

b. With an example explain verilog synthesis information extraction from module inputs and outputs. **(04 Marks)**

c. Write VHDL / verilog code for signal assignment statement Y = (2* x + 3) for an entity with one input X of 2-bits and one output Y of 4-bits. Show mapping of this signal assignment to gate level. **(12 Marks)**

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06EC45

Fourth Semester B.E. Degree Examination, Dec.09-Jan.10
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the structure of VHDL module and Verilog module. (05 Marks)

b. Given A = 1000 and B = 0011, perform the following operations :
   i) AXNOR B
   ii) Shift B two position left logical
   iii) Reduction NAND
   iv) Verilog concatenation {A, B}
   v) Verilog modulus A % B. (05 Marks)

c. Explain the Verilog data types. (04 Marks)

d. List the types of descriptions. Write VHDL code to describe one bit full adder using mixed style description. (06 Marks)

2 a. What are the facts of data flow description? Explain with an example the execution of signal assignment statement in HDL. (06 Marks)

b. Derive a minimized Boolean function of the system that has three 1 bit input 'a' and 1 bit output 'b'. The output 'b' is '1' when input 'a' is 1, 3, 6, 7, otherwise 'b' is 'O'. Write a dataflow description in VHDL. What is the function of this system? (04 Marks)

c. Write the block diagram of a 4 bit ripple carry adder and its Boolean functions. Write a dataflow description in verilog. Assume 3 ns propagation delay for all two input gates. Draw the simulation waveform. (10 Marks)

3 a. Explain the execution of process statement. (02 Marks)

b. Distinguish between :
   i) VHDL IF and VHDL case
   ii) VHDL Next and Exit
   iii) Verilog repeat and Verilog forever
   iv) Always and initial. (08 Marks)

c. Using Booth algorithm, find the product of two 4 bit numbers -3 and 8. Write a Verilog code using behavioral style of description. (10 Marks)

4 a. Explain how binding is achieved in VHDL between :
   i) Entity and component
   ii) Library and module (04 Marks)

b. Write a VHDL structural description of a full adder using two half adder and an OR gate. Write the simulation waveform. (08 Marks)

c. Write a Verilog structural description of a N = 3 bit magnitude comparator using generate statement. (08 Marks)

PART – B

5 a. What are the significance of procedure, tasks and functions? Differentiate between procedure/task and function. (04 Marks)

b. Write a code to convert the unsigned integer to (N = 4) binary using procedure. (08 Marks)

c. Write a VHDL code for finding the word with the lowest ASCII value using file operations. (08 Marks)

6 a. Explain the implementation of single dimensional and two dimensional arrays in VHDL. (04 Marks)

b. Write a block diagram and function table of 128 x 16 static memory. Write a Verilog code. Verify the code by simulation waveform by writing data in memory locations 8, 18, 46, 126 and read the contents of two memory locations 18 and 46. (08 Marks)

c. Explain the fetch and execute cycles of basic computer for the following operations :
Halt, Add, Mult, NAND. (08 Marks)

7 a. Write mixed-language description of a master slave D flip flop invoking a VHDL entity from a Verilog module. (10 Marks)

b. Write a mixed-language description of an AND gate invoking a Verilog module from a VHDL module. (06 Marks)

c. What are the limitations of mixed-language descriptions? (04 Marks)

8 a. What is synthesis? List the general steps involved in synthesis. (08 Marks)

b. Give synthesis information extracted, when the input and output are defined as :
i) bit ii) Std – logic – vector. (04 Marks)

c. Write a behavioral code in VHDL and Verilog for the signal assignment statement Y = X. Explain the mapping to gate level logic diagram. (08 Marks)

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06EC45

Fourth Semester B.E. Degree Examination, May/June 2010
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the behavioral and structural description types of HDL programming, with examples and keywords used. **(10 Marks)**

b. Explain the following data types:
i) Physical std_logic and bit_vector in VHDL
ii) Nets, parameters and registers in verilog. **(10 Marks)**

2 a. How do you assign a delay time to the signal assignment statement? Explain the dataflow model of 2×1 multiplexer in VHDL and verilog. **(10 Marks)**

b. Explain the use of data type vectors with dataflow description of 2×2 unsigned combinational array multiplier in VHDL and verilog. **(10 Marks)**

3 a. Differentiate between signal and variable assignment statement in VHDL. Write VHDL programs for behavioral description of D-latch using signal assignment and variable assignment. **(10 Marks)**

b. Explain the formats of for-loop and while-loop statements in VHDL and verilog. **(06 Marks)**

c. Write verilog description for a 4-bit priority encoder. **(04 Marks)**

4 a. Explain the binding in the following, with example:
i) Between entity and component in VHDL
ii) Between two modules in verilog. **(10 Marks)**

b. Write the HDL programs for N+1 bit magnitude comparator using
i) generate and generic in VHDL ii) generate and parameter in verilog. **(10 Marks)**

PART – B

5 a. Explain the use of procedure (in VHDL) and task (in verilog) with description of full adder, using half adders. **(10 Marks)**

b. Explain the file declaration and built in procedures for file handling in VHDL. **(10 Marks)**

6 a. How to attach a package to the VHDL module? Explain with an example. **(08 Marks)**

b. What is the need of mixed type descriptions? Write description of 16×8 SRAM in VHDL and verilog. **(12 Marks)**

7 a. How to imvoke a VHDL entity from a verilog module. Explain with an example. **(10 Marks)**

b. Write a HDL program for mixed language descriptions of a JK-flip-flop with a clear input. **(10 Marks)**

8 a. Write a flow diagram of synthesis. Explain its steps. **(08 Marks)**

b. Write VHDL code for signal assignment statement y = 2 * x + 3. Show the synthesized logic symbol and gate level diagram. Write structural code in verilog using the gate level diagram. **(12 Marks)**

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